Q.P. Code: 19EC0433 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech IV Year I Semester Regular Examinations November/December-2022

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Illustrate the steps involved in NMOS fabrication process with neat sketches.	L2	6M
	b	Discuss about body bias effect in the NMOS transistor.	L1	6M
		OR		
2	a	Determine the relationship between I_{ds} & V_{ds} in non-saturated region.	L3	6M
	b	Explain in detail about Transconductance.	L2	6M

UNIT-II

3	a	Explain the steps involved in VLSI Design flow.	L2	6M
	b	Explain about Stick diagram with one example.	L2	6M
		OR		
4	a	Explain 2μm design rules for contacts and transistors.	L2	6M
	b	Sketch the layout diagram for CMOS inverter.	L3	6M

UNIT-III

5	a	Draw the CMOS implementation of 4X1 mux using transmission gates.	L1	6M
	b	Explain pseudo NMOS logic gate?	L2	6M
		OR		
6	a	What are the design methods used in physical design cycle? Explain each term with suitable diagrams.	L1	6M
	b	What is routing? Explain about different routing techniques?	L2	6M

UNIT-IV

7		Design an Arithmetic and Logic Unit circuit with four functions using multiplexers and explain its operation.	L3	12M
		OR		
8	a	Construct and explain the circuit diagram of 4-bit Ripple Carry Adder.	L3	4M
	b	Construct and explain the ripple counter.	L3	4M
	c	Explain about 4 transistor Dynamic memory cell.	L2	4M

UNIT-V

9	a	Illustrate the architecture of FPGA with neat sketch.	L2	6M
	b	Discuss about the merits of FPGA over other PLD architectures.	L2	6M
		OR		
10	a	What is the need for testing? Explain about Fault simulation.	L1	6M
	b	Give a logic circuit example in which stuck-at-1 fault and stuck-at-0 fault are indistinguishable.	L2	6M

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